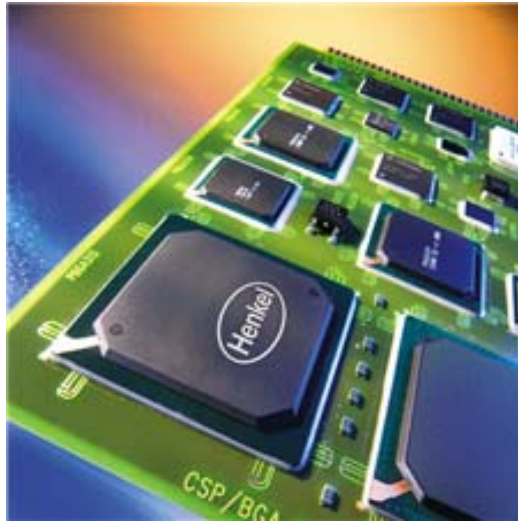




## Technologies



### **Enhancing Pb-free Solder Joint Reliability**

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When the electronics industry first began to discuss the mandatory move to lead-free manufacturing, it was widely believed that the transition would also enable more reliable solder joints. Bulk testing of tin-silver-copper systems showed increased strength, which should deliver joints with higher strength—most notably creep strength—as compared to SnPb solder joints. However, with certain package types, lead-free assemblies seem to be more vulnerable to failures. To find out why, one must examine why a solder joint fails and then analyze how to amend the problem.

The factors that affect solder joint reliability must be evaluated first to determine how reliable a lead-free solder joint is likely to be once in the field. Generally speaking, the usual failure for a good solder joint is Low Cycle Fatigue (LCF), which is when differential thermal expansion through temperature cycling or power cycling puts continuous stress on the joint until it fails. While flaws in the material can cause LCF failures, one must remember that solder joints do have a finite life and will fail after a certain number of cycles. As stated above, if the bulk properties of a solder alloy were used as the main indicator of solder joint reliability, it would seem logical that lead-free assemblies should have higher reliability, but that's not the case. So, clearly, the bulk alloy tests are an insufficient guide for lead-free assembly reliability. Therefore, other factors such as design and process dynamics must be evaluated to fully understand lead-free solder joint reliability. Design factors would include things such as component and PCB size and composition as well as an analysis of how the board is populated. Understanding these issues will help determine the pattern of stress applied to individual joints. Likewise, process conditions must also be evaluated and variables such as alloy composition, reflow and cooling profiles, solder paste characteristics and stencil design must be considered.

Through research conducted by technical experts at Henkel, data shows that lead-free solder joints in area array components are more vulnerable to failures due to CTE

(coefficient of thermal expansion) mismatches. The lower ductility of the lead-free alloys along with the increased likelihood of assembly warpage due to the higher peak reflow temperatures are among the primary causes for these failures. And, as we move to finer pitched devices and thinner substrates, the situation will become more problematic.

Some creep in the solder joint is advantageous so that the joint can absorb the forces arising from CTE mismatches. When this is absent, joints are prone to cracking. However, there are exceptions and some devices such as SOICs and QFPs are more resistant to this than others. In the case of these two package types, the component leads are able to flex and cracking of the joint due to board warpage is minimized. Chip-type components, though, have a tendency to show fractures in the joint on one side of the component after only 2000 thermal shock cycles.

Moving to the wafer level, however, these effects are less easily observed or understood. Direct-attach CSPs that encompass a large area and experience broad temperature fluctuations during normal use have reduced lead-free joint reliability. And, as CSP devices continue the drive toward miniaturization with increasing numbers of interconnects, finer pitches and smaller solder ball diameters, the solder joint area and relational standoff will make the effects of CTE mismatches even more significant. In addition, as more CSPs are being used on portable devices, which are subjected to drop vibration and stress, reliability with respect to this stress also needs to be considered.

In order to enhance the reliability of these lead-free CSP devices, assemblers should contemplate the use of underfills, which will distribute stress across the entire surface of the substrate so that solder bumps are less subjected to concentrated stresses and, therefore, failures. Though CSPs were designed to be underfill-free assemblies, the move to lead-free manufacturing and the resulting brittleness of the solder joints particularly in area array packages has made underfilling these devices the most cost-effective and viable solution for enhancing reliability.

Not all underfills are suitable, however, and electronics assemblers must carefully evaluate which materials are most appropriate for their lead-free applications. The correct underfill needs to be selected based on the component and the reliability required. There are certain types of underfills which are designed to withstand the higher lead-free reflow temperature of 260°C without any material degradation during subsequent reflow and can be used for Pb-free CSP assembly without any modifications. But, in the case of no-flow underfills, a dedicated lead-free formulated material should be used, as traditional no-flow underfills have a cure behavior that allows for component self-alignment. During reflow, if the underfill cures too early during the profile, no self-alignment will occur and yield will be reduced. So, a no-flow material optimized for Pb-free processes is imperative.

Certainly, more research into the failure vulnerability of various CSP packages is required to fully understand when underfill materials are necessary to enhance the Pb-free reliability of these packages. But, regardless of the increased functionality and miniaturization demands for these packages, customers and end-users still expect them to be reliable even when assembled in a lead-free process. The use of certain types of underfills can do much to enhance the reliability of these critical devices.

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